UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,379	02/12/2004	Iwen Chao	110348-135995	8999

31817 7590 09/28/2006

SCHWABE, WILLIAMSON & WYATT
PACWEST CENTER, SUITE 1900
1211 S.W. FIFTH AVE.
PORTLAND, OR 97204

EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,379	CHAO, IWEN	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4 and 6-34* is/are pending in the application.

4a) Of the above claim(s) *16-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-15 and 31-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed July 13, 2006 has been entered. Claims 1 and 15 have been amended. Claims 1, 3, 4 and 6-34 are pending. Non-elected invention, claims 16-30 have been withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1, 3, 4, 6-15 and 31-34 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "wherein the low resistive path barrier surrounds the conductivity region **to further isolate the conductivity region and the semiconductor device from the deep trench isolation**" in the application as filed.

At best, the specification, page 7, lines 7-8, discloses: "A low resistive path barrier 152 surrounds the conductivity region 156 **isolating the conductivity region 156 from the underlying substrate 158**.

Applicant must provide support or cancel the new matter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 4, 7, 10, 13, 14, 31, 32 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Chu et al. (U.S. Patent No. 5,015,594)).

With respect to claim 1, as best understood by the examiner, Chu teaches an apparatus as claimed including:

a semiconductor device formed on a conductivity region (14), the conductivity region (14) comprises a first type doping material (N) having a first doping concentration; a low resistive path barrier (12) formed surrounding the conductivity region (14) to isolate the conductivity region (14) from a substrate (10) that supports the conductivity region (14) and the low resistive path barrier (12), the low resistive path barrier (12) comprises the first type doping material (N) having a second doping concentration (N^+), wherein the second doping concentration (N^+) is greater than the first doping concentration (N);

a deep trench isolation (20) formed surrounding the low resistive path barrier (12) on the opposite side of the conductivity region (14); and

wherein the semiconductor device is selected on of CMOS, BiCMOS, NMOS and PMOS; and

wherein the low resistive path barrier (12) surrounds the conductivity region (14) to further isolate the conductivity region and the semiconductor device from the underlying substrate (10). (See Fig. 19).

With respect to claim 3, the deep trench isolation (20) of Chu extend into the substrate (10).

With respect to claim 4, the conductive region (14) of Chu is at least one of n-type and p-type conductivity regions.

With respect to claim 7, the substrate (10) of Chu is selected from one of p-type and n-type substrate.

With respect to claim 8, the low resistive path barrier (12) of Chu comprises of a plug (28) coupled to a buried layer (12).

With respect to claim 10, the low resistive path barrier (12) of Chu comprises a selected one of N+ and P+ doped material.

With respect to claim 11, the deep trench isolation of Chu comprises of a selected one of a dielectric and an insulation material.

With respect to claim 13, the low resistive path barrier (12) of Chu comprises a first capacitive decoupling junction located at an interface between the low resistive path barrier (12) and the conductivity region (14), and a second capacitive decoupling junction located at an interface between the low resistive path barrier (12) and the substrate (10).

With respect to claim 14, the (N^+) low resistive path barrier (12) and the plug (28) of Chu having doping concentration of E19-E20 atoms/cm^3 , thus, resistivity as claimed.

With respect to claim 31, the first type doping material (N) of Chu has a first doping concentration is an n type doping material (14), and the first type doping material having a second doping concentration is an n+ type doping material (12).

With respect to claim 32, the conductive region (14) of Chu further comprises a second type doping material (14B) having a third doping concentration (P^-), the second type doping material being a P type doping material, and the third doping concentration (P^-) being lesser than the second doping concentration (N^+).

With respect to claim 34, the second doping concentration (N^+) of Chu is about ten times that of the first doping concentration (N). This is common knowledge in the art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 4, 6-11, 13, 31, 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellul et al. (U.S. Patent No. 5,614,750) in view of Hsu (U.S. Patent No. 4,975,764) of record.

With respect to claim 1, as best understood by the examiner, Ellul teaches an apparatus as claimed including:

a semiconductor device (90) formed on a conductivity region (57), the conductivity region (57) comprises a first type doping material having a first doping concentration (n); and

a low resistive path barrier (55) formed surrounding the conductivity region (57) to isolate the conductivity region (57) from a substrate (52) that supports the conductivity region (57) and the low resistive path barrier (55), the low resistive path barrier (55) comprises the first type doping material having a second doping concentration (n^+), wherein the second doping concentration (n^+) is greater than the first doping concentration (n)

a deep trench isolation (68) formed surrounding the low resistive path barrier (55) on the opposite side of the conductivity region; and

wherein the semiconductor device is a bipolar; and

wherein the low resistive path barrier (55) surrounds the conductivity region (57) to further isolate the conductivity region (57) and the semiconductor device (90) from the underlying substrate (52). (See Figs. 6-7).

Thus, Ellul is shown to teach all the features of the claim with the exception of the semiconductor device is a selected one of CMOS, BiCMOS, NMOS and PMOS.

However, Hsu teaches a bipolar semiconductor device can be formed in a BiCMOS circuit because it offers the possibility of higher density with lower power consumption than is typically found in bipolar circuit. (See col. 1, lines 14-37).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the apparatus of Ellul in conjunction with CMOS device, thus, BiCMOS as taught by Hsu to lower power consumption in a higher density circuit.

With respect to claim 3, the deep trench isolation (68) of Ellul extends into the substrate.

With respect to claim 4, the conductive region (57) of Ellul is at least one of n-type and p-type conductivity regions.

With respect to claim 6, in view of Hsu, the low resistive path barrier (150) is coupled to electrical connection (132), hence power supply.

With respect to claim 7, the substrate (52) of Ellul is selected from one of p-type and n-type substrate.

With respect to claim 8, the low resistive path barrier (52) of Ellul comprises of a plug (82) coupled to a buried layer (55).

With respect to claim 9, in view of Hsu, the plug (108) is coupled to electrical connection (132), hence power supply.

With respect to claim 10, the low resistive path barrier (55) of Ellul comprises a selected one of N+ and P+ doped material.

With respect to claim 11, the deep trench isolation (68) of Ellul comprises of a selected one of a dielectric and an insulation material.

With respect to claim 13, the low resistive path barrier (55) of Ellul comprises a first capacitive decoupling junction located at an interface between the low resistive path barrier (55) and the conductivity region (57), and a second capacitive decoupling junction located at an interface between the low resistive path barrier (55) and the substrate (52).

With respect to claim 31, the first type doping material of Ellul has a first doping concentration is an n type doping material, and the first type doping material having a second doping concentration is an n+ type doping material.

With respect to claim 32, in view of Hsu, the conductive region further comprises a second type doping material (107) having a third doping concentration (P), the second type doping material being a P type doping material, and the third doping concentration (P) being lesser than the second doping concentration (N^+).

With respect to claim 34, the second doping concentration (n^+) of Ellul is about ten times that of the first doping concentration (n). This is common knowledge in the art.

5. Claim 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu '594 as applied to claims 1 and 8 above, and further in view of Tomassetti (U.S. Patent No. 4,825,275) of record.

Chu teaches the low resistive path barrier is coupled to interconnect (106).

Thus, Chu is shown to teach all the features of the claim with the exception of explicitly disclosing the interconnect is to a power supply.

However, Tomassetti teaches the low resistive path barrier is coupled to the most positive voltage applied to the chip, thus, power supply. (See col. 5, ll. 20-24).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to couple the low resistive path barrier of Chu to the power supply as taught by Tomassetti since the subcollector is well known to connect to supply voltage.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chu or Ellul and Hsu as applied to claim 1 above, and further in view of Takeuchi et al. (U.S. Patent No. 5,939,755) of record.

Chu or Ellul and Hsu are shown to teach all the features of the claim with the exception of explicitly disclosing the substrate is biased to 0 volts. Note that, the claimed biased to 0 volts does not appear to be critical since the Applicant has admitted that the substrate may be biased to the highest or lowest voltage.

However, Takeuchi teaches the substrate (11) may be biased to 0 volts (grounded). (See Figs. 2, 7, 9).

Note that the specification contains no disclosure of either the *critical nature of the claimed biased to 0 volts* of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to bias the substrate of Chu or Ellul and Hsu to 0 volts (ground) as taught by Takeuchi to avoid latchup.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ellul and Hsu as applied to claim 8 above, and further in view of Hoshi et al. (U.S. Patent No. 5,635,742) of record.

Ellul and Hsu teach the apparatus as described in claim 8 above including: the low restive path barrier (55) and a plug (82), wherein both plug and barrier layer are heavily doped (N^+). Note that the claimed resistivity do not appear to be critical.

Thus, Ellul and Hsu are shown to teach all the features of the claim with the exception of explicitly disclosing the dopant concentration, thus, the resistivity of the plug and barrier layer.

However, Hoshi teaches an apparatus having a low resistive path barrier (2/7) surrounding a conductivity region (4), wherein the low resistive path barrier (2/7) comprises a plug (7) coupled to a buried layer (2) having dopants concentration of $5x10^{17}$ to $1x10^{20}$ cm^{-3} and $5x10^{17}$ to $1x10^{21}$ cm^{-3}, respectively. (See Fig. 2, col. 4, lines 9-32).

Note that the specification contains no disclosure of either the *critical nature of the claimed resistivity of the plug and the buried layer* of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the plug and buried layer of Tomassetti or Ellul to have the dopant concentrations as taught by Hoshi to isolate conductive region from the substrate.

Note that, the resistivity are determined by the dopant concentration. Since the dopant concentration of Hoshi encompasses the dopant concentration of the instant plug and buried layer, thus, encompasses the claimed (resistivity) range.

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chu or Ellul and Hsu as applied to claim 1 above, and further in view of Desko et al. (U.S. Pub. No. 2003/0211701) of record.

Chu or Ellul teaches the apparatus as described in claim 1 above including deep trench isolation (20) extends into the substrate (10) and below the low resistive barrier (12).

Thus, Chu or Ellul are shown to teach all the features of the claim with the exception of explicitly disclosing the depth of the deep trench. Note that, the claimed depth of 5 μm does not appear to be critical.

However, Desko teaches deep trench isolation (310) is formed into substrate (220) to a depth of 5 μm to 8 μm. (See Fig. 3).

Note that the specification contains no disclosure of either the *critical nature of the claimed depth of* 5μm of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the deep trench isolation of Chu or Ellul into the substrate to the depth as taught by Desko to isolate the apparatus from the adjacent devices.

9. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chu or Ellul and Hsu, as applied to claim 1 above , and further in view of Lee et al. (U.S. Patent No. 5,278,084).

Chu or Ellul and Hsu teach an apparatus as described above including: the first type doping material having a first doping concentration (14) and the first type doping material having a second doping concentration (12).

Thus, Chu or Ellul and Hsu are shown to teach all the features of the claim with the exception of utilizing P type dopant for the first type doping material.

However, Lee teaches a similar BiCMOS apparatus including the first type doping material having a first doping concentration (27) utilizing p type doping material and the first type doping material having a second doping concentration (21) utilizing P^+ type doping material.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the first type doping material having first and second doping concentration of Chu or Ellul and Hsu to include P type dopant (P and P^+) as taught by Lee to isolate one type of device (PMOS) form the other (NMOS).

Response to Arguments

10. Applicant's arguments filed July 13, 2006 have been fully considered but they are not persuasive.

Rejection under 35 U.S.C. 102 and 103

Applicant argues that the collector layer 12 does not "surround" the semiconductor device **to isolate the semiconductor device from the deep trench isolation 20** as currently recited in claim 1.

Applicant argues about the new limitation that does not have adequate support. As discussed above, this is **new matter** and must be cancelled.

All rejection are therefore, maintained.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER